ABSTRACT OF THE DISCLOSURE

A data memory circuit is provided. In one embodiment, the data memory circuit comprises a plurality of addressable memory cells, a command decoding device for decoding external commands and a control device for controlling or initiating operations for the operation of the data memory circuit in each case in a manner dependent on the decoded commands. The memory circuit has critical operating states in which the execution of specific commands is impermissible resulting in the course of specific operations in the data memory circuit, wherein a command buffer device buffer-stores commands received during the duration of their impermissibility and releases them for execution after the end of their impermissibility.